Customer Training Workshop

Traveo™ II Time Division Multiplexed (TDM)/ Inter-IC sound (I^2S) Interface

Q4 2020

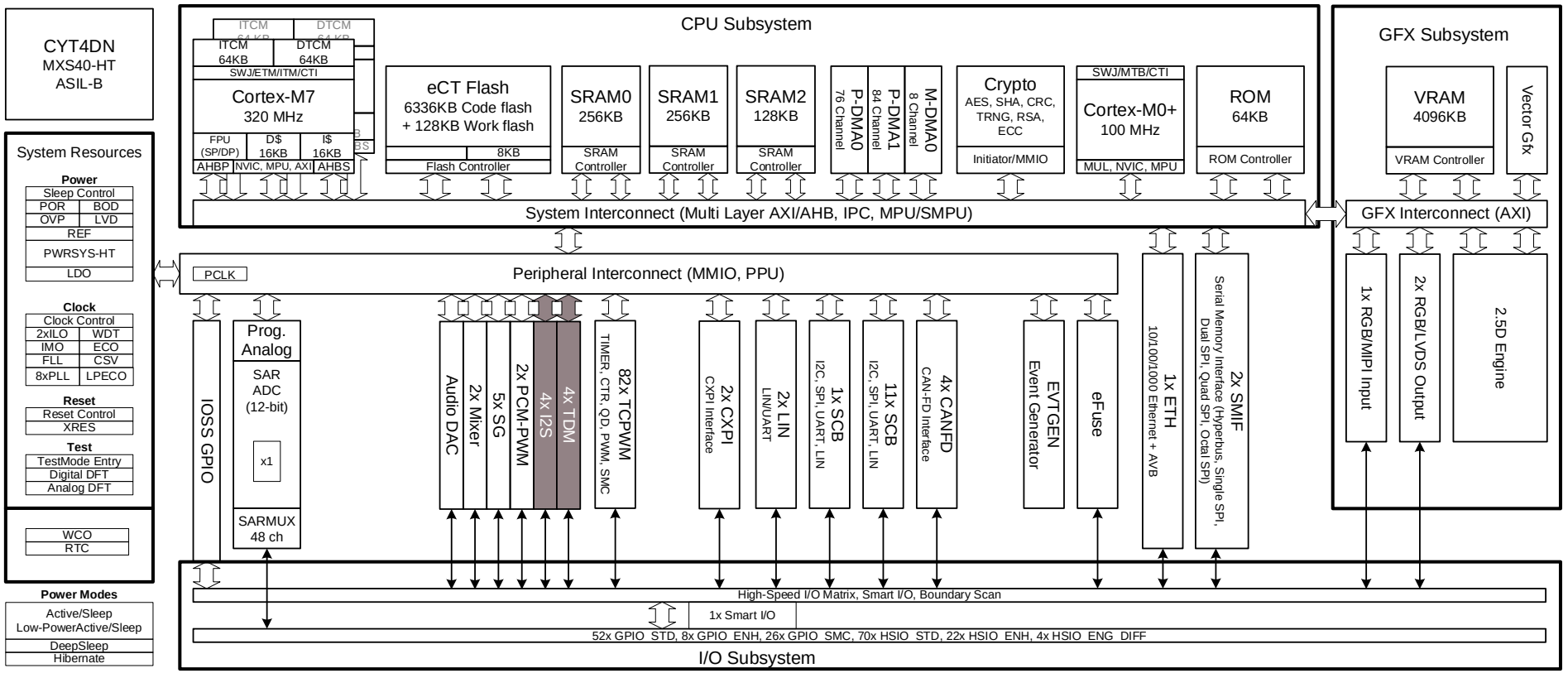
Target Products

- Target product list for this training material:

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Cluster	CYT3DL	Up to 4160KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336KB

Introduction to Traveo II Cluster

- Time Division Multiplexed (TDM) / Inter-IC sound (I^2S) Interface is part of Peripheral blocks



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Review TRM chapter 33 for additional details

Introduction to TDM/I²S Interface

- Overview
  - TDM/I²S interface consists of a TDM transmitter and a TDM receiver, which can function with multiple channels simultaneously. I²S interface is obtained as a special case of TDM.
- Features
  - Combined I²S and TDM functionality
  - Master and slave functionality
  - Full-duplex transmitter and receiver operation
  - Support for up to 32 channels
  - Programmable interface clock
  - Programmable channel size (up to 32 bits)
  - Programmable late capture extra delay of 1, 2 or 3 cycles
  - Delayed sampling support
  - Programmable Pulse Code Modulation (PCM) sample formatting (8, 10, 12, 14,16, 18, 20, 24, and 32 bits)
  - Left-aligned and right-aligned sample formatting
  - 128-entry TX and RX FIFOs with interrupt and trigger support

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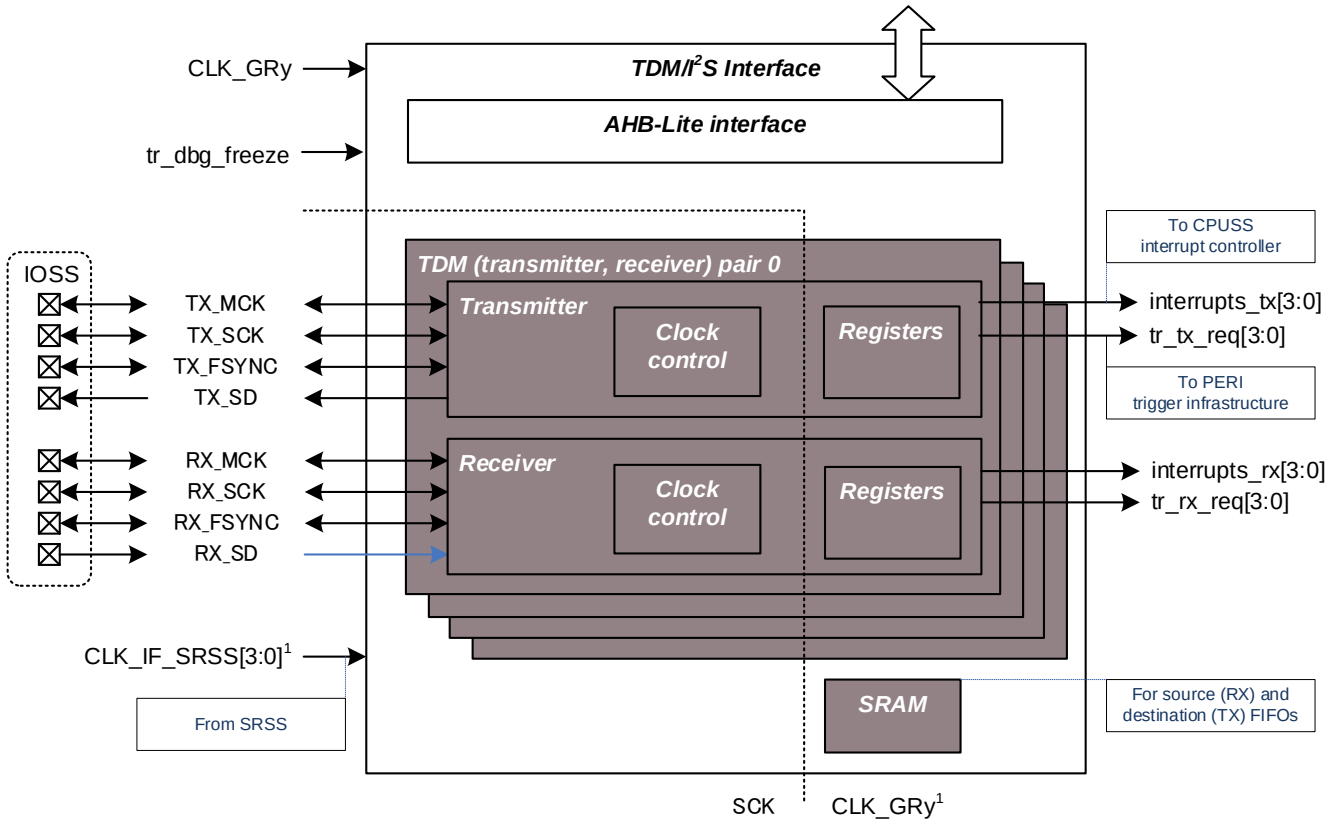
Review TRM section 33.2 for additional details

Block Diagram

- TDM/I²S components
  - TDM/I²S interface
    - Clock
    - TDM/I²S pair (transmitter, receiver)
    - SRAM



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Review TRM section 33.2.2 for additional details

SRSS clock (CLK_IF_SRSS[3:0]) is dependent on the device

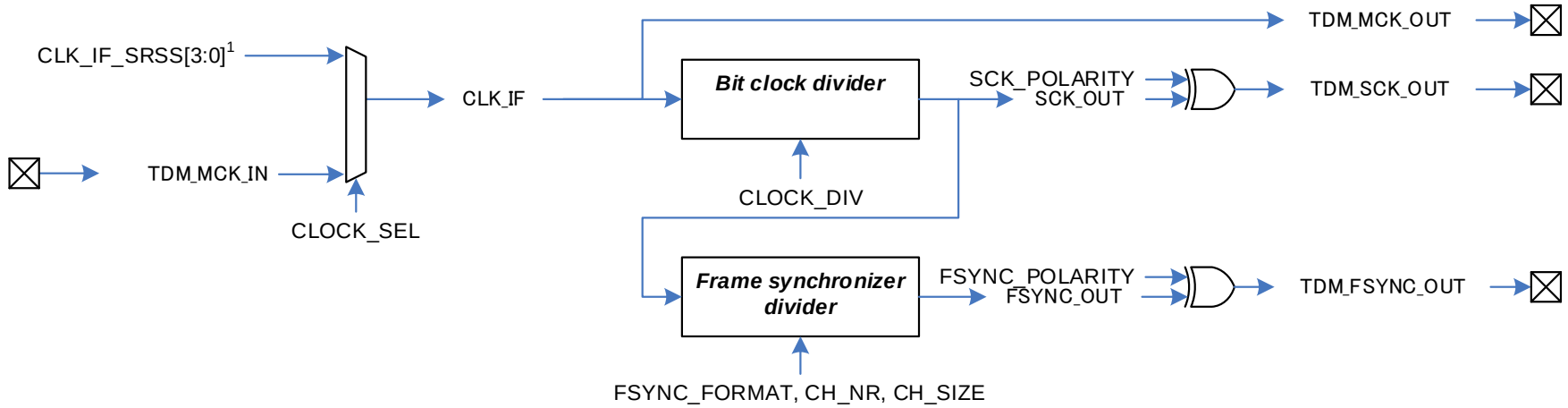
CLK_GR: Clock input to peripheral functions

Clock

- TDM/I²S interface clock can be derived from either of these clock signals

Signal	Description
CLK_IF_SRSS[3:0][1]	SRSS clock
TDM_MCK_IN	Master clock input

- An interface clock (CLK_IF) is derived and then gated to derive the TDM clock



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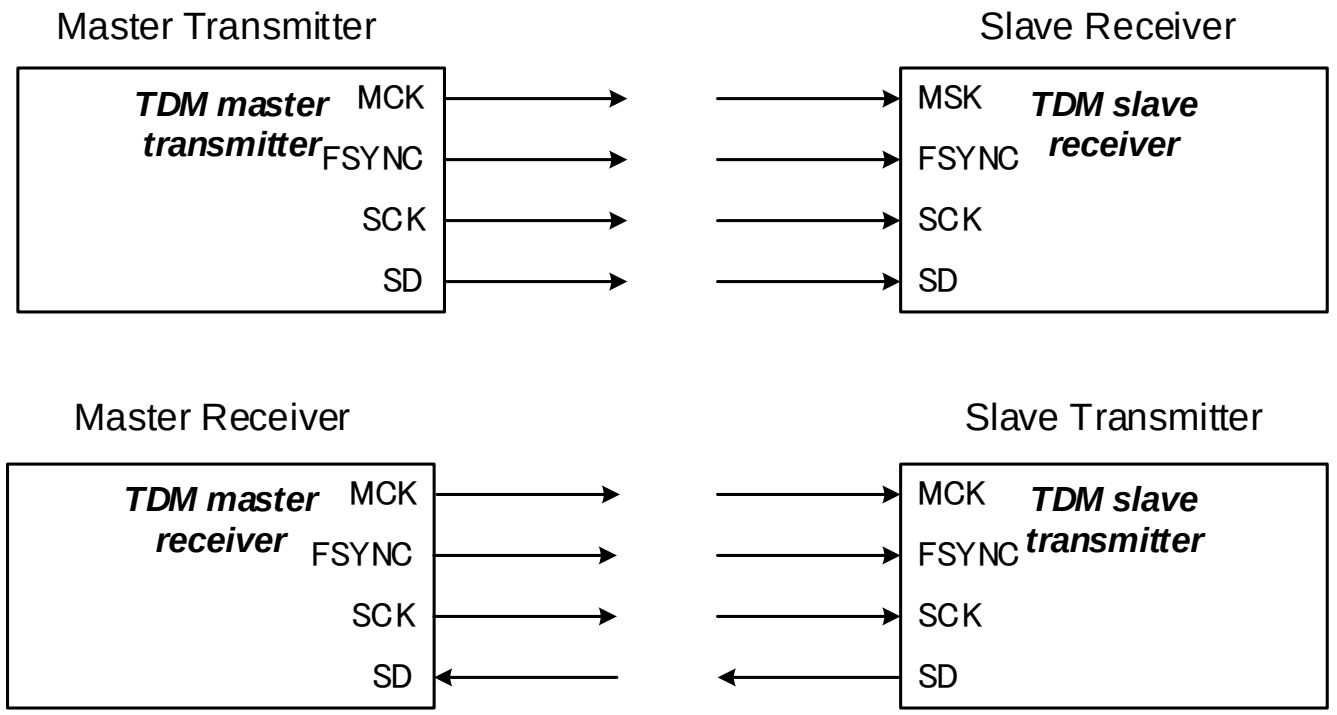
Review TRM section 33.2.5 for additional details

Review the Clock System Training section for additional details about high-frequency clocks

[1] Note: See the device datasheet for assigned clocks to CLK_IF_SRSS[3:0] and CLK_GRy.

Operation Modes

- Each TDM transmitter and receiver can be configured independently
- Masters output the TDM clock and Frame synchronization; slaves take the same signals as inputs



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Review TRM section 33.2.3 for additional details

I²S Modes

- When the below programming is applied, the transmitter operates according to the I²S protocol:
  - Number of channels equal 2:
    - TDMx_TDM_STRUCTy_TDM_TX_STRUCT_TX_IF_CTL.CH_NR = 1
  - FSYNC format over the channel:
    - TDMx_TDM_STRUCTy_TDM_TX_STRUCT_TX_IF_CTL.FSYNC_FORMAT = 1
  - FSYNC polarity inverted:
    - TDMx_TDM_STRUCTy_TDM_TX_STRUCT_TX_IF_CTL.FSYNC_POLARITY = 1
  - I²S mode setting:
    - TDMx_TDM_STRUCTy_TDM_TX_STRUCT_TX_IF_CTL.I2S_MODE = 1
- The receiver also operates according to the I²S protocol:
  - For RX the below register programmed:
    - TDMx_TDM_STRUCTy_TDM_RX_STRUCT_RX_IF_CTL.

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Review TRM section 33.2.4 for additional details

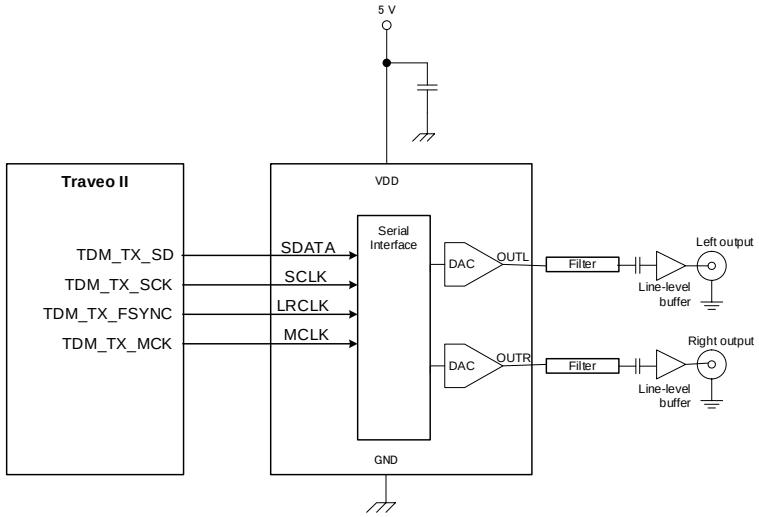
In I²S mode, “word select” signaling is absolved by TDM_TX_FSYNC or TDM_RX_FSYNC

Master Clock Output

- TDM_TX_MCK is derived from the fractional PLL to support typical external clock rate for an external audio codec

Sampling Rate (Fs) [kHz]	Master Clock Frequency (TDM_TX_MCK) [MHz]		
	TDM_TX_MCK / Fs = 256	TDM_TX_MCK / Fs = 384	TDM_TX_MCK / Fs = 256
32	8.1920	12.2280	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

- Master Clock Output Signal for the External Audio Codec



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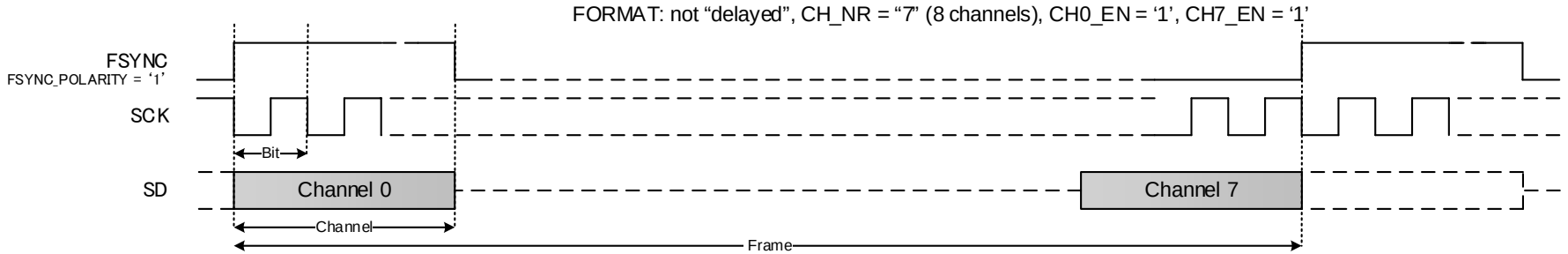
Review TRM section 33.2.6 for additional details

Transfer Format

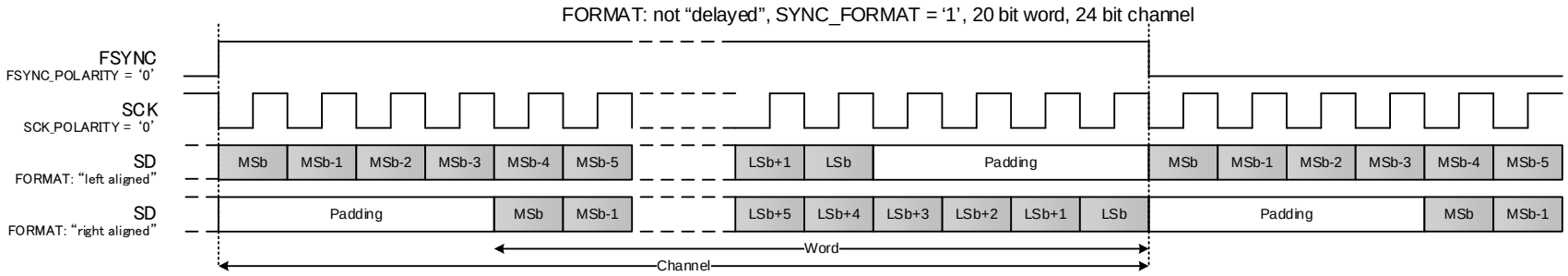
- Example: Transfer for eight channels, with only channels 0 and 7
  - Channels can be enabled individually



- Example: 24-bit Channel Size and 20-bit Word Size Format
  - PCM data word size is potentially smaller than the channel size
  - PCM data word is either left-aligned or right-aligned within the channel

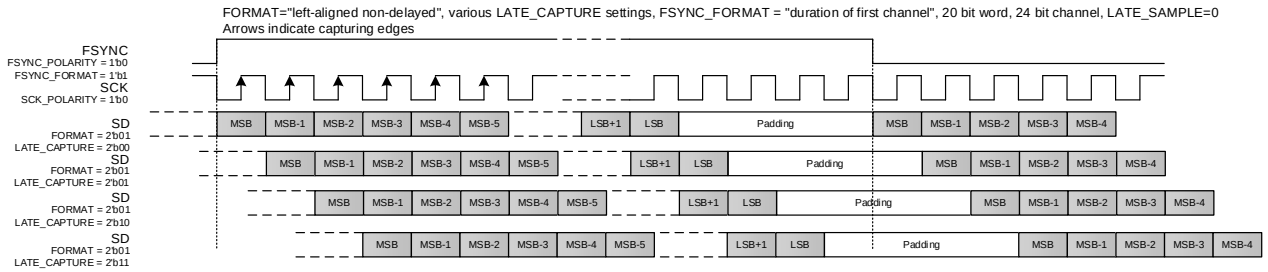
If the data word is left-aligned, a receiver ignores the trailing four bits in the channel

If the data word is right-aligned, a receiver ignores the leading four bits in the channel

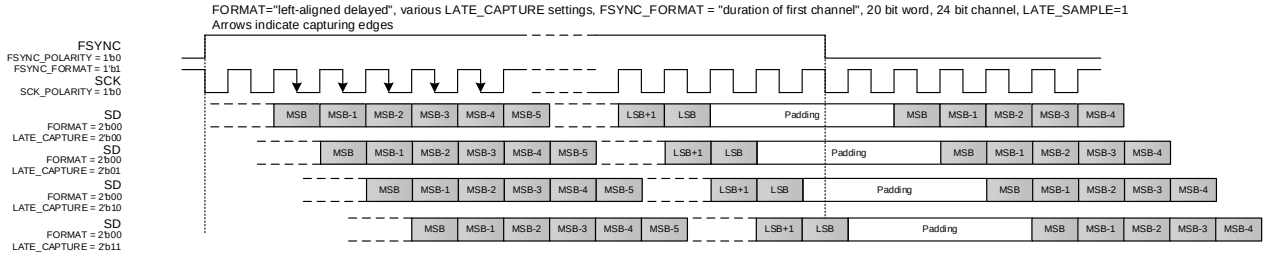


Late Capture

- The TDM/I²S interface supports a programmable extra delay:
  - Pushes out the capturing edges used by the receiver to sample TDM_RX_SD
  - Intended to support very large round-trip delays in a master receiver configuration
  - The timing diagrams below illustrate how the receiver interprets the bits of the received TDM frame
    - Late Capture with Non-delayed Format and Late Sample = 0



    - Late Capture with Delayed Format and Late Sample = 1



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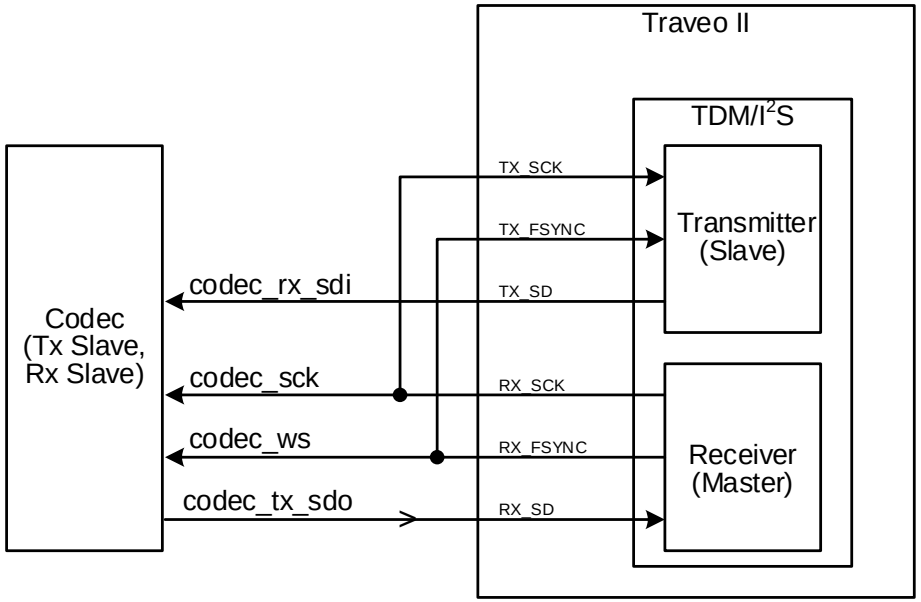
Review TRM section 33.2.8 for additional details

Interfacing with Audio Codecs having Common WS and SCK Signals

- Connections for Codecs with separate WS and SCK signals for RX and TX directions



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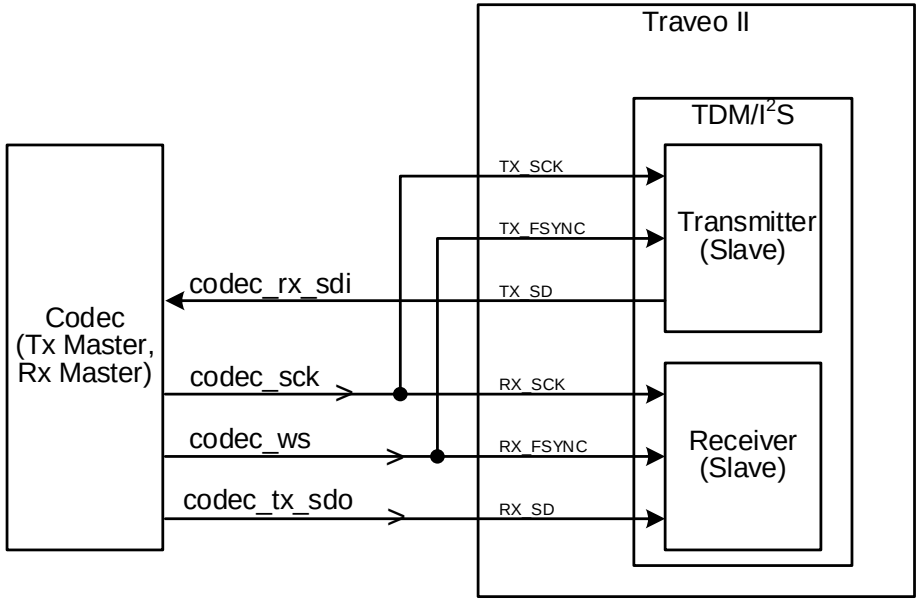

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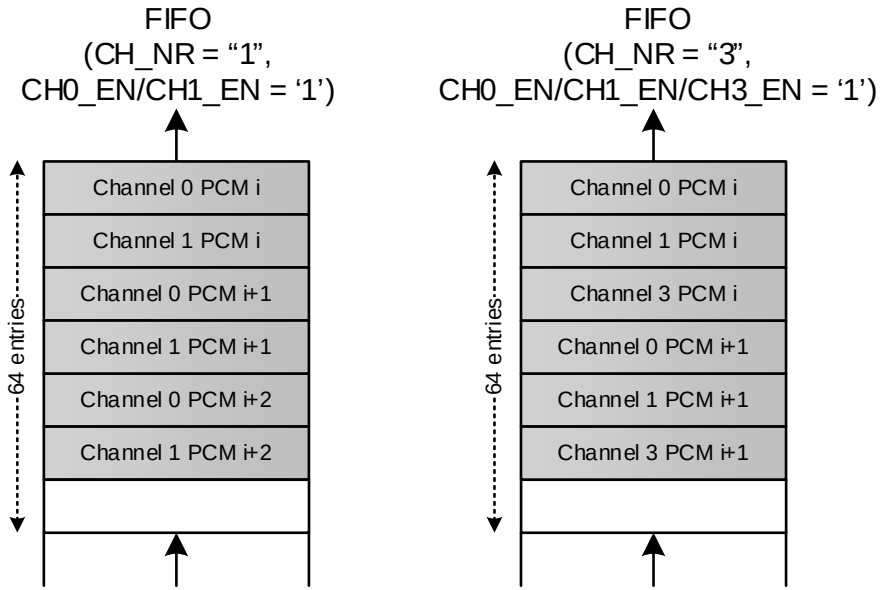
Review TRM section 33.2.9 for additional details

FIFO

- The transmitter and receiver have a dedicated FIFO
  - Common SRAM is used for all TX and RX FIFOs; each FIFO uses 128 32-bit entries
  - Transmitter transmits PCM words from the TX FIFO and a receiver receives PCM words into the RX FIFO
  - It is possible to enable/disable the individual channels within a frame
  - Disabled channels do not have PCM words in the FIFOs
  - When multiple channels are enabled, the channels have their PCM words interleaved in the FIFOs



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Review TRM section 33.2.10 and Register TRM for additional details

Interrupt

› The following events trigger a TDM interrupt:

TX Interrupt	Set Condition
FIFO_TRIGGER	TX trigger is generated.
FIFO_OVERFLOW	Writing to a full TX FIFO (TX_FIFO_STATUS.USED is “128”).
FIFO_UNDERFLOW	Reading from an almost empty TX FIFO (TX_FIFO_STATUS.USED < “number of enabled channels per frame”).
IF_UNDERFLOW[1]	PCM samples are generated too fast by the interface logic. May indicate that the IP system frequency is too low with respect to the interface frequency (a SW configuration error).

RX Interrupt	Set Condition
FIFO_TRIGGER	RX trigger is generated.
FIFO_OVERFLOW	Writing to an almost full RX FIFO (128 -RX_FIFO_STATUS.USED < “number of enabled channels per frame”).
FIFO_UNDERFLOW	Reading from an empty RX FIFO (RX_FIFO_STATUS.USED is “0”).
IF_UNDERFLOW[1]	PCM samples are generated too fast by the interface logic. May indicate that the IP system frequency is too low with respect to the interface frequency (a SW configuration error).

[1] This functionality is for debug purposes

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Review Register TRM for additional details

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002-28407 *B, 2020-12-24

Revision History

Revision	ECN	Submission Date	Description of Change
**	6677245	09/18/2019	Initial release
*A	6809284	02/18/2020	Added note descriptions in each slide
*B	7053683	12/24/2020	Updated page 2, 3, 4, 5, 6, Added 8, 9, 11, 12